# Spin-based quantum computing using silicon-MOS quantum dots

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Spin qubits in silicon are excellent candidates for scalable quantum information processing [1] due to their long coherence times and the enormous investment in silicon CMOS technology. In particular, gate-defined quantum dots formed using standard silicon metal-oxide-semiconductor (SiMOS) technology [2] can be conveniently configured to realise multi-qubit devices. Such qubits can have long spin lifetimes T1 = 2 s, while electric field tuning of the conduction-band valley splitting removes problems due to spin-valley mixing [3]. In isotopically enriched Si-28 these SiMOS qubits have demonstrated control fidelities exceeding 99% using simple pulsed electron spin resonance (ESR) [4], while more sophisticated optimized ESR pulses enable fidelities exceeding 99.9%, consistent with that required for fault-tolerant QC. By gate-voltage tuning the electron g-factor, the ESR operation frequency can be Stark shifted by > 10 MHz [4], allowing individual addressability of many qubits. Neighbouring SiMOS quantum dot qubits can also be directly exchange coupled, and a CNOT gate can be realised by a combination of single qubit rotations and a two-qubit CZ operation [5]. Now that both one- and two-qubit logic are available in silicon, one of the next challenges on the path to large-scale quantum computing will be the demonstration of quantum error correction protocols, to realize a logical qubit which can have a coherence time much longer than its constituent physical qubits. A recent paper [6] has proposed a detailed design and protocol for a logical qubit based on a linear array of silicon quantum dots, comprising between 14 and 20 spins. I will conclude my talk by discussing the prospects of scalability of this technology using traditional CMOS manufacturing, in order to realise large-scale 2D arrays of potentially millions of qubits [7].

[1] D.D. Awschalom et al., “Quantum Spintronics”, *Science* 339, 1174 (2013).

[2] S.J. Angus et al., “Gate-defined quantum dots in intrinsic silicon”, *Nano Lett.* 7, 2051 (2007).

[3] C.H. Yang et al., “Spin-valley lifetimes in a silicon quantum dot with tunable valley splitting”, *Nature Comm.* 4, 2069 (2013).

[4] M. Veldhorst et al., “An addressable quantum dot qubit with fault-tolerant control fidelity”, *Nature Nanotechnology* 9, 981 (2014).

[5] M. Veldhorst et al., “A two-qubit logic gate in silicon”, *Nature* 526, 410 (2015).

[6] Cody Jones et al., “A logical qubit in a linear array of semiconductor quantum dots”, arXiv:1608.06335.

[7] M. Veldhorst et al., “Silicon CMOS architecture for a spin-based quantum computer”, arXiv:1609.09700, to appear in *Nature Communications*.

**Acknowledgments.** We acknowledge support from the US Army Research Office (W911NF-13-1-0024 and W911NF-17-1-0198), the Australian Research Council (CE11E0001017), and the NSW Node of the Australian National Fabrication Facility. The views and conclusions contained in this document are those of the author and should not be interpreted as representing the official policies, either expressed or implied, of the Army Research Office or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Government purposes notwithstanding any copyright notation herein.